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1. A digital computer has a memory unit of 64K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.
2. How many bits are there in the tag, block and word fields of the address format?
3. How many blocks can the cache accommodate?

**Solution-**

64 K × 16: 16 bit address; 16-bit data.

1. 6 8 2 = 16 bits address

|  |  |  |
| --- | --- | --- |
| TAG | BLOCK | WRD |

1. 28 = 256 blocks of 4 words each

2. Consider a fully associative mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find number of bits in tag and word fields.

3. Consider a 2-way set associative mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find number of bits in tag , set and word fields.

4. Consider a direct mapped cache with 8 cache blocks (0-7). If the memory block requests are in the order-

3, 5, 2, 8, 0, 6, 3, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24

Which of the following memory blocks will be in the cache at the end of the sequence? Also, calculate the hit ratio and miss ratio.

We have,

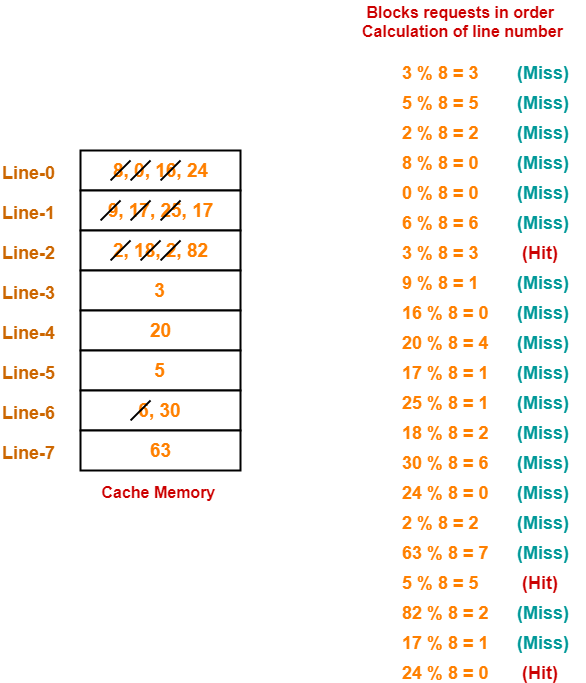
* There are 8 blocks in cache memory numbered from 0 to 7.
* In direct mapping, a particular block of main memory is mapped to a particular line of cache memory.
* The line number is given by-

Cache line number = Block address modulo Number of lines in cache

**Solution-**

For the given sequence-

* Requests for memory blocks are generated one by one.
* The line number of the block is calculated using the above relation.
* Then, the block is placed in that particular line.
* If already there exists another block in that line, then it is replaced.



* Hit ratio = 3 / 21
* Miss ratio = 18 / 21

5. Consider a fully associative cache with 8 cache blocks (0-7). The memory block requests are in the order-

4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7

If LRU replacement policy is used, which cache block will have memory block 7?

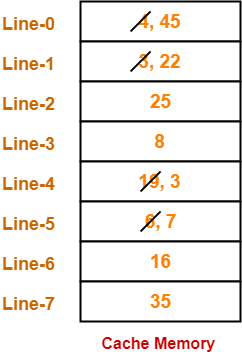
Also, calculate the hit ratio and miss ratio.

**Solution-**

We have,

* There are 8 blocks in cache memory numbered from 0 to 7.
* In fully associative mapping, any block of main memory can be mapped to any line of the cache that is freely available.
* If all the cache lines are already occupied, then a block is replaced in accordance with the replacement policy.

4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7



Thus,

* Line-5 contains the block-7.
* Hit ratio = 5 / 17
* Miss ratio = 12 / 17

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6. Consider a system with 2 level caches. Access times of Level 1 cache, Level 2 cache and main memory are 1 ns, 10ns, and 500 ns, respectively. The hit rates of Level 1 and Level 2 caches are 0.8 and 0.9, respectively. What is the average access time of the system ignoring the search time within the cache?

Average access time = [H1 \*T1 ]+ [ (1 -H1 ) \* H2 \*T2 ]+ [ (1 -H1 ) (1 -H2 ) \*Tm ]

Where,

H1 = Hit rate of level 1 cache = 0.8

T1 = Access time for level 1 cache = 1 ns

H2 = Hit rate of level 2 cache = 0.9

T2 = Access time for level 2 cache = 10 ns

Tm = Access time for Main Memory = 500 ns

So, Average Access Time = (0.8 \* 1 ) + ( 0.2 \* 0.9 \* 10 ) + ( 0.2 \* 0.1 \* 500)

= 0.8 + 1.8 + 10

= 12.6 ns